Electronic Version
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Claims

[c1] 1. A method of generating an accurate scan enable signal when testing an integrated circuit using a sequential scanning technique, wherein said sequential scanning technique is designed to operate said integrated circuit in a scan mode if said accurate scan enable signal is at a first logic level and in a capture mode if said accurate scan enable signal is at a second logic level, said method comprising:
receiving a first scan enable signal having a first transition from said first logic level to said second logic level and a second transition from said second logic level to said first logic level; and
generating said accurate scan enable signal from said first scan enable signal by timing said first transition to be synchronous with a clock signal, and passing said second transition on said accurate scan enable signal asynchronously.

[c2] 2. The method of claim 1, wherein said clock signal is used to clock a plurality of memory elements contained in said integrated circuit, said clock signal containing a plurality of low speed clock pulses in which a scan se-

quence is scanned into said plurality of memory elements in said scan mode, said clock signal further containing a plurality of high speed clock pulses in which said integrated circuit is operated in said capture mode.

[c3] 3. The method of claim 2, wherein said first scan enable signal is received from a test equipment, wherein said first transition of said first scan enable signal is received before a rising edge of a first high speed clock pulse, and said second transition is received after said plurality of high speed clock pulses, wherein said first high speed clock pulse is contained in said plurality of high speed clock pulses.

[c4] 4. A presettable circuit generating an accurate scan enable signal when testing an integrated circuit using a sequential scanning technique, wherein said sequential scanning technique is designed to operate said integrated circuit in a scan mode if said accurate scan enable signal is at a first logic level and in a capture mode if said accurate scan enable signal is at a second logic level, said presettable circuit comprises:
a flip-flop containing a preset input and an output, wherein said preset input is coupled to receive a first scan enable signal and said output is coupled to provide said accurate scan enable signal, whereby said accurate scan enable signal transitions to said first logic level

asynchronously.

[c5] 5. The presettable circuit of claim 4, said flip-flop further contains a data input and a clock input, wherein said data input and said clock input receive said first scan enable signal and a clock signal respectively, whereby said accurate scan enable signal transitions to said second logic level synchronously.

[c6] 6. The presettable circuit of claim 5, wherein said clock signal is used to clock a plurality of memory elements contained in said integrated circuit, said clock signal containing a plurality of low speed clock pulses in which a scan sequence is scanned into said plurality of memory elements in said scan mode, said clock signal further containing a plurality of high speed clock pulses in which said integrated circuit is operated in said capture mode.

[c7] 7. The presettable circuit of claim 7, wherein said first scan enable signal is received from a test equipment, wherein said first transition of said first scan enable signal is received before a rising edge of a first high speed clock pulse, and said second transition is received after said plurality of high speed clock pulses, wherein said first high speed clock pulse is contained in said plurality of high speed clock pulses.

[c8] 8. The presettable circuit of claim 5, wherein said flip-flop comprises a D flip-flop.

[c9] 9. A gating circuit generating an accurate scan enable signal when testing an integrated circuit using a sequential scanning technique, wherein said sequential scanning technique is designed to operate said integrated circuit in a scan mode if said accurate scan enable signal is at a first logic level and in a capture mode if said accurate scan enable signal is at a second logic level, said gating circuit comprises:

a flip-flop receiving a first scan enable signal as an input and being clocked by a clock signal, whereby transitions on an output of said flip-flop are synchronous with said clock signal; and

a logic gate receiving said first scan enable signal as a first input and said output of said flip-flop as another input, said logic gate generating said accurate scan enable signal as said output, said logic gate passing said first logic level received on said first scan enable signal to said output such that said accurate scan enable signal transitions asynchronously to said first logic level, and whereby transitions to said second logic level are synchronous with said clock signal.

[c10] 10. The gating circuit of claim 9, wherein said logic gate comprises an OR gate.

[c11] 11. The gating circuit of claim 10, wherein said flip-flop comprises a D-flop.

[c12] 12. The gating circuit of claim 9, wherein said clock signal is used to clock a plurality of memory elements contained in said integrated circuit, said clock signal containing a plurality of low speed clock pulses in which a scan sequence is scanned into said plurality of memory elements in said scan mode, said clock signal further containing a plurality of high speed clock pulses in which said integrated circuit is operated in said capture mode.

[c13] 13. The gating circuit of claim 11, wherein said first scan enable signal is received from a test equipment, wherein said first transition of said first scan enable signal is received before a rising edge of a first high speed clock pulse, and said second transition is received after said plurality of high speed clock pulses, wherein said first high speed clock pulse is contained in said plurality of high speed clock pulses.

[c14] 14. An apparatus generating an accurate scan enable signal when testing an integrated circuit using a sequential scanning technique, wherein said sequential scanning technique is designed to operate said integrated circuit in a scan mode if said accurate scan enable signal

is at a first logic level and in a capture mode if said accurate scan enable signal is at a second logic level, said apparatus comprising:

means for receiving a first scan enable signal having a first transition from said first logic level to said second logic level and a second transition from said second logic level to said first logic level; and

means for generating said accurate scan enable signal from said first scan enable signal by timing said first transition to be synchronous with a clock signal, and passing said second transition on said accurate scan enable signal asynchronously.

[c15] 15. The apparatus of claim 14, wherein said clock signal is used to clock a plurality of memory elements contained in said integrated circuit, said clock signal containing a plurality of low speed clock pulses in which a scan sequence is scanned into said plurality of memory elements in said scan mode, said clock signal further containing a plurality of high speed clock pulses in which said integrated circuit is operated in said capture mode.

[c16] 16. The apparatus of claim 15, wherein said first scan enable signal is received from a test equipment, wherein said first transition of said first scan enable signal is received before a rising edge of a first high speed clock pulse, and said second transition is received after said

plurality of high speed clock pulses, wherein said first high speed clock pulse is contained in said plurality of high speed clock pulses.

[c17] 17. An integrated circuit comprising:
a combinational logic generating a plurality of outputs based on a plurality of inputs;
a plurality of memory elements connected in sequence and being clocked by a clock signal, each of said plurality of memory elements operable in a scan mode or a capture mode according to an accurate scan enable signal, wherein a scan sequence is scanned into said plurality of memory elements as said plurality of inputs in said scan mode and said plurality of outputs are captured in said capture mode; and
a generation circuit receiving a first scan enable signal containing a first transition from said scan mode to said capture mode and a second transition from said capture mode to said scan mode, said generation circuit generating said accurate scan enable signal with said first transition being timed to be synchronous with said clock signal and with said second transition being asynchronous.

[c18] 18. The integrated circuit of claim 17, wherein said clock signal contains a plurality of low speed clock pulses and a plurality of high speed clock pulses, wherein said inte-

grated circuit is operated in said capture mode in a time duration corresponding to said high speed clock pulses and in said scan mode in a time duration corresponding to said low speed clock pulses.

[c19] 19. The integrated circuit of claim 18, wherein said first scan enable signal is received from a test equipment, wherein said first transition of said first scan enable signal is received before a rising edge of a first high speed clock pulse, and said second transition is received after said plurality of high speed clock pulses, wherein said first high speed clock pulse is contained in said plurality of high speed clock pulses.